WE CLAIM

1. An integrated circuit for performing data processing, said integrated circuit comprising:

a plurality of processing stages, a processing stage output signal from at least one processing stage being supplied as a processing stage input signal to a subsequent processing stage, wherein said at least one processing stage comprises:

processing logic operable to perform a processing operation upon at least one coded input value to generate a processing logic output signal, said coded input value being an input value to which an error correction code has been applied;

a non-delayed signal-capture element operable to capture a non-delayed value of said processing logic output signal at a non-delayed capture time, said non-delayed value being supplied to said subsequent processing stage as said processing stage output signal following said non-delayed capture time;

a delayed signal-capture element operable to capture a delayed value of said processing logic output signal at a delayed capture time, later than said non-delayed capture time;

error correction logic operable to detect an occurrence of a random error in said delayed value of said processing logic output signal, to determine if said detected random error is correctable using said error correction code and to either generate an error-checked delayed value or to indicate that said detected random error is not correctable;

a comparator operable to compare said non-delayed value with said error-checked delayed value to detect a change in said processing logic output signal at a time following said non-delayed capture time, said change being indicative of a systematic error whereby said processing logic has not finished said processing operation at said non-delayed capture time or of a random error in said non-delayed value; and

error-repair logic operable when said comparator detects said change in said processing logic output signal to perform an error-repair operation suppressing use of said non-delayed value either by replacing said non-delayed value by said error-checked delayed value in subsequent processing stages or by initiating repetition of said processing operation and processing operations of subsequent processing stages

if said error correction logic indicates that said detected random error is not correctable.

2. An integrated circuit as claimed in claim 1, wherein said error repair logic is operable to suppress use of said non-delayed value by replacing said non-delayed value with said error-checked delayed value in the event that said error correction logic detects a correctable random error in said delayed value and said comparator detects that there is no difference between said non-delayed value and said error-checked delayed value.

3. An integrated circuit as claimed in claim 1, wherein said processing operation performed by said processing logic is an operation for which said processing logic output signal is substantially equal to said processing stage input value when no errors occur in said processing operation.

4. An integrated circuit as claimed in claim 3, wherein said at least one processing stage is performed by a memory circuit and said processing operation is a read or write operation.

5. An integrated circuit as claimed in claim 3, wherein at least one processing stage is performed by a register and said processing operation is a read, write or move operation.

6. An integrated circuit as claimed in claim 3, wherein said at least one processing stage is performed by a multiplexer and said processing operation is a multiplexing operation.

7. An integrated circuit as claimed in claim 1, wherein said plurality of processing stages are respective pipeline stages within a synchronous pipeline.

8. An integrated circuit as claimed in claim 3, wherein said input value is error correction encoded using a Hamming code and said error repair logic performs said correction and said detection using said Hamming code.

9. An integrated circuit as claimed in claim 1, wherein said processing operation performed by said processing logic is a value-altering operation for which said processing logic output signal can be different from said processing stage input value even when no errors occur in said processing operation.

10. An integrated circuit as claimed in claim 9, wherein said processing logic is one of: an adder, a multiplier or a shifter.

11. An integrated circuit as claimed in claim 8, wherein said input value is error correction encoded using an arithmetic code comprising one of: an AN code, a residue code, an inverse residue code or a residue number code.

12. An integrated circuit as claimed in claim 1, comprising a meta-stability detector operable to detect meta-stability in said non-delayed value and trigger said error-repair logic to suppress use of said non-delayed value if found to be meta-stable.

13. An integrated circuit as claimed in claim 1, wherein when said comparator detects said change said error-repair logic is operable to replace said non-delayed value with said error-checked delayed value as said processing stage output signal.

14. An integrated circuit as claimed in claim 13, wherein supply of said error-checked delayed value to said following processing stage forces forward progress through processing operations.

15. An integrated circuit as claimed in claim 1, wherein when said comparator detects said change said error-repair logic is operable to force said error-checked delayed value to be stored in said non-delayed signal-capture element in place of said non-delayed value.

16. An integrated circuit as claimed in claim 1, wherein processing operations within said at least one processing stage and said subsequent processing stages are driven by a non-delayed clock signal.

17. An integrated circuit as claimed in claim 16, wherein when said comparator detects said change said error-repair logic is operable to gate said non-delayed clock signal to provide time for said following processing stage to recover from input of said non-delayed value and instead use said error-checked delayed value.

18. An integrated circuit as claimed in claim 16, wherein said non-delayed capture time is derived from a predetermined phase point of said non-delayed clock signal, a phased delayed version of said non-delayed clock signal is used as a delayed clock signal and said delayed capture time is derived from a predetermined phase point of said delayed clock signal.

19. An integrated circuit as claimed in claim 1, wherein one or more operating parameters of said integrated circuit are controlled in dependence upon detection of said systematic errors corresponding to said change.

20. An integrated circuit as claimed in claim 19, wherein said one or more operating parameters are controlled to have a level at which a non-zero systematic error rate is maintained.

21. An integrated circuit as claimed in claim 19, wherein said one or more operating parameters include at least one of:

an operating voltage;
an operating frequency;
an integrated circuit body bias voltage; and
temperature.

22. An integrated circuit as claimed in claim 1, wherein a minimum processing time taken for said processing operation is greater than a time separating said delayed capture time from said non-delayed capture time such that said error-checked delayed value is not influenced by a processing operation performed upon different input values.

23. An integrated circuit as claimed in claim 22, wherein said processing logic includes one or more delay elements to ensure said minimum processing time is exceeded.

24. An integrated circuit as claimed in claim 1, wherein a maximum processing time taken for said processing operation is less than a sum of a time separating said delayed capture time from said non-delayed capture time and a time between non-delayed capture times such that said processing logic will have completed said processing operation by said delayed capture time.

25. An integrated circuit as claimed in claim 1, wherein said processing stages are part of a data processor.

26. An integrated circuit as claimed in claim 1, comprising an error counter circuit operable to store a count of detection of errors corresponding to said change.

27. An integrated circuit as claimed in claim 26, wherein said count may be read by software.

28. A method of controlling an integrated circuit for performing data processing, said method comprising the steps of:

supplying a processing stage output signal from at least one processing stage of a plurality of processing stages as a processing stage input signal to a subsequent processing stage, said at least one processing stage operating to:

perform a processing operation with processing logic upon at least one coded input value to generate a processing logic output signal, said coded input value being an input value to which an error correction code has been applied;

capturing a non-delayed value of said processing logic output signal at a non-delayed capture time, said non-delayed value being supplied to said subsequent processing stage as said processing stage output signal following said non-delayed capture time;

capturing a delayed value of said processing logic output signal at a delayed capture time later than said non-delayed capture time;

detect an occurrence of a random error in said delayed value of said processing logic output signal using error correction logic, to determine if said detected random error is correctable using said error correction code and to either generate an error-checked delayed value or to indicate that said detected random error is not correctable;

comparing said non-delayed value with said error-checked delayed value to detect a change in said processing logic output signal at a time following said non-delayed capture time, said change being indicative of a systematic error whereby said processing logic has not finished said processing operation at said non-delayed capture time or of a random error in said non-delayed value; and

when said change is detected, performing an error-repair operation using error-repair logic suppressing use of said non-delayed value either by replacing said non-delayed value by said error-checked delayed value in subsequent processing stages or by initiating repetition of said processing operation and processing operations of subsequent processing stages if said error correction logic indicates that said detected random error is not correctable.

29. A method as claimed in claim 28, wherein said error repair logic is operable to suppress use of said non-delayed value by replacing said non-delayed value with said error-checked delayed value in the event that said error correction logic detects a correctable random error in said delayed value and said comparator detects that there is no difference between said non-delayed value and said error-checked delayed value.

30. A method as claimed in claim 1, wherein said processing operation performed by said processing logic is an operation for which said processing logic output signal is substantially equal to said processing stage input value when no errors occur in said processing operation.

31. A method as claimed in claim 30, wherein said at least one processing stage is performed by a memory circuit and said processing operation is a read or write operation.

32. A method as claimed in claim 30, wherein at least one processing stage is performed by a register and said processing operation is a read, write or move operation.

33. A method as claimed in claim 30, wherein said at least one processing stage is performed by a multiplexer and said processing operation is a multiplexing operation.

34. A method as claimed in claim 1, wherein said plurality of processing stages are respective pipeline stages within a synchronous pipeline.

35. A method as claimed in claim 30, wherein said input value is error correction encoded using a Hamming code and said error repair logic performs said correction and said detection using said Hamming code.

36. A method as claimed in claim 1, wherein said processing operation performed by said processing logic is a value-altering operation for which said processing logic output signal can be different from said processing stage input value even when no errors occur in said processing operation.

37. A method as claimed in claim 36, wherein said processing logic is one of: an adder, a multiplier or a shifter.

38. A method as claimed in claim 36, wherein said input value is error correction encoded using an arithmetic code comprising one of: an AN code, a residue code, an inverse residue code or a residue number code.

39. A method as claimed in claim 1, comprising a meta-stability detection in said non-delayed value and triggering of said error-repair logic to suppress use of said non-delayed value if found to be meta-stable.

40. A method as claimed in claim 28, wherein when said change is detected by said comparator said error-repair logic is operable to replace said non-delayed value with said error-checked delayed value as said processing stage output signal.

41. A method as claimed in claim 28, wherein supply of said error-checked delayed value to said following processing stage forces forward progress through processing operations.

42. A method as claimed in claim 28, wherein when said change is detected by said comparator, said error-repair logic is operable to force said error-checked delayed value to be stored in said non-delayed signal-capture element in place of said non-delayed value.

43. A method as claimed in claim 28, wherein processing operations within said at least one processing stage and said subsequent processing stages are driven by a non-delayed clock signal.

44. A method as claimed in claim 43, wherein when said change is detected by said comparator, said error-repair logic is operable to gate said non-delayed clock signal to provide time for said following processing stage to recover from input of said non-delayed value and instead use said error-checked delayed value.

45. A method as claimed in claim 43, wherein said non-delayed capture time is derived from a predetermined phase point of said non-delayed clock signal, a phased delayed version of said non-delayed clock signal is used as a delayed clock signal and said delayed capture time is derived from a predetermined phase point of said delayed clock signal.

46. A method as claimed in claim 28, wherein one or more operating parameters of said integrated circuit are controlled in dependence upon detection of said systematic errors corresponding to said change.

47. A method as claimed in claim 47, wherein said one or more operating parameters are controlled to have a level at which a non-zero systematic error rate is maintained.

48. A method as claimed in claim 46, wherein said one or more operating parameters include at least one of:

an operating voltage;
an operating frequency;
an integrated circuit body bias voltage; and
temperature.

49. A method as claimed in claim 28, wherein a minimum processing time taken for said processing operation is greater than a time separating said delayed capture time from said non-delayed capture time such that said error-checked delayed value is not influenced by a processing operation performed upon different input values.

50. A method as claimed in claim 49, wherein said processing logic includes one or more delay elements to ensure said minimum processing time is exceeded.

51. A method as claimed in claim 28, wherein a maximum processing time taken for said processing operation is less than a sum of a time separating said delayed capture time from said non-delayed capture time and a time between non-delayed capture times such that said processing logic will have completed said processing operation by said delayed capture time.

52. A method as claimed in claim 28, wherein said processing stages are part of a data processor.

53. A method as claimed in claim 28, comprising an error counter circuit operable to store a count of detection of errors corresponding to said change.

54. A method as claimed in claim 53, wherein said count may be read by software.